A New 6 GHz fully integrated Low Power Low Phase Noise CMOS LC Quadrature VCO

Jae-Hong Chang [1], Yong-Sik Youn [2], Mun-Yang Park [2] and Choong-Ki Kim [1]

[1]Department of EECS, Korea Advanced Institute of Science and Technology (KAIST),

373-1, Guseong-Dong, Yuseong-Gu, Daejeon, 305-701, Republic of Korea

[2]Elcctronics and Telecommunications Research Institute (ETRI),

Gajeong-Dong, Yuseong-Gu, Daejeon, 305-350, Republic of Korea
E-mail: *rfcmos@mail.kaist.ac.kr*, TEL: +82-42-869-8016

Abstract — **A new fully integrated low power and low phase noise 6 GHz quadrature VCO is designed and fabricated in standard commercial 0.18 μm single-poly, 6-metal CMOS process. The one VCO-core draws only 1.6mA of current from a 1.8V supply. Total power consumption - include two VCO-cores and two VCO-buffers - for generating quadrature signal is 18mW. Measured phase noise at 1 MHz offset from the center frequency is –115 dBc/Hz. It has tuning range of 1.2 GHz with low phase noise performance throughout the tuning range. It meets the requirements for IEEE802.11a and HiperLAN type 2 standards. Low power and low phase noise have been achieved simultaneously by the use of new proposed cascode coupling topology.**

I. INTRODUCTION

Increasing pressure for low power, small volume, low cost, and reduced bill of materials in such radio applications as mobile communications has driven academia and industry to resurrect the Direct Conversion Receiver (DCR). Also CMOS RF, with its mature technology, low fabrication cost and high packing density is recognized as the only suitable material satisfying the needs of the rapidly growing communication market, i.e. IEEE 802.11a, Bluetooth, and WCDMA etc [1], [2]. One of the most beneficial merits of CMOS process is the continuous scaling down. Thus the sub-micron gate length MOSFETs can be used for low-noise applications at microwave frequencies (f_T = 50 GHz) [3].

The very important and hardly integrated sub-block is VCO in CMOS process. The key performance parameter of VCO is phase noise. Generally in other RF standards, such as cellular, WCDMA has very stringent phase noise specification. This stringent spec makes integrate VCO on chip difficult. In IEEE802.11a and HiperLAN type 2 have more some released phase noise specification [4], [5], [6]. From standards of above systems, the phase noise performance is at least –112 dBc/Hz @ 1MHz offset.

The frequency band of IEEE802.11a and HiperLAN type 2 have the same lower band 5.15 ~ 5.35 GHz on the contrary to upper band in 5.7 ~ 5.8 GHz at IEE802.11a, 5.4 ~ 5.7 GHz at HiperLAN type 2. To meet the two standards (IEEE802.11a & HiperLAN type2), the VCO has large tuning range about 1 GHz.

DCR can translate RF signal to baseband without any other intermediate frequency which is the common method used in superheterodyne. DCR is the best system architecture to integrat on chip radio receiver. But DCR has well known problem, such as DC offset, 1/f noise, and IQ mismatch [7]. To overcome IQ mismatch, this paper propose new quadrature VCO. This VCO has new coupling scheme to acquire high accurate IQ signal, low power, and low phase noise.

This paper is organized as follow: In section II, we describe the performance of the used variable capacitor which is the key component in VCO; section III discuss the new VCO topology and VCO's buffer, section IV presents measurement results and section V concludes the paper.

II. DESCRPTION OF VARACTOR

A conventional standard 0.18 μm 1P6M CMOS technology was used to fabricate various structures for varactor. We have used MOS accumulation varactors with n+ contacts in n-well. For RF circuitry, a very important circuit element is the tunable LC-tank, which in the simplest case consists only of an inductor and a varactor. The tunable LC-tank can be used for RF filtering and RF VCO's. In both cases it is essential to have a high quality factor Q. As spiral inductors are preferred over bondwire inductors and thick metal inductor, due to process

0-7803-7694-3/03/$17.00 © 2003 IEEE

simplicity and cost, the limiting factor on Q is the inductor. In a standard CMOS process spiral inductors with a Q of 10 are hard to make, if no impossible. Typical values ranges from 3 to 6. Consequently a lot of work has been published on inductor, while varactors seems to be more or less overlooked. In the ideal case a varactor should have both a very large capacitance ratio and a very high Q. This paper proposes new varactor structure.

Fig. 1 and Fig. 2 show the new surrounding ground varactor layout and its equivalent physical parasitics in the silicon substrate.

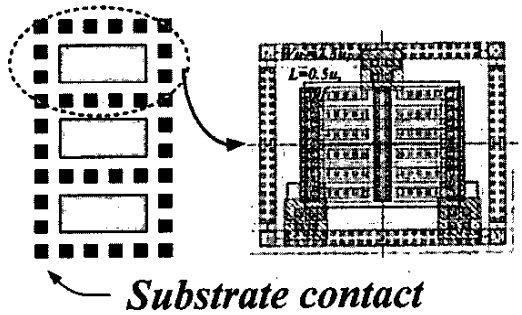

Fig. 1. New surrounding ground varactor layout (Accumulation MOS varactor)

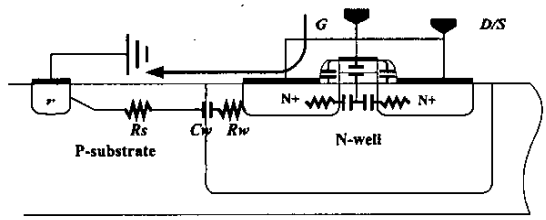

Fig. 2. Physical parasitics in silicon substrate

Generally, typical varactor used in CMOS was not clearly defined substrate contact [8]. This may caused the serious loss in RF signal pass through the gate of the MOS varactor to the substrate. Fig. 1 shows the new proposed varactor layout. This is named surrounding ground varactor. Surrounding ground decreased the substrate loss which is modeled by Rs in Fig. 2. Many Active device used in RF circuits used this layout technique already [9].

Fig. 3 shows the measured and simulated Q. The nominal capacitance (in the condition of zero gate voltage) 1.2pF shows the maximum Q ~ 130 at 1GHz.

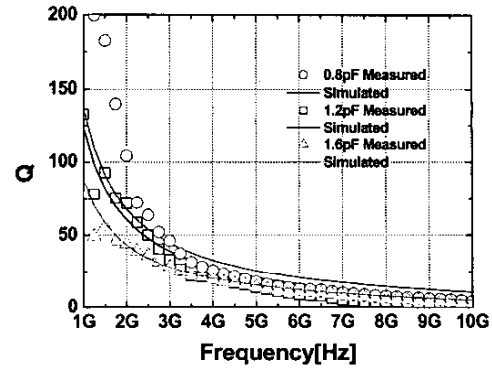

Fig. 3. Measured and simulated Q of proposed varactor

III. PROPOSED NEW QUADRATURE VCO

Typical quadrature generation method is shown in Fig.4. Two cross couple VCO core can generate quadrature signal [10]. The role of coupling MOS is to make pi/4 phase difference between I (in-phase signal node) and Q (quadrature-phase signal node). As shown in Fig. 4, the coupling MOS has two performance degradation effects. Firstly, the coupling MOS require additional current. Secondly, the typical VCO is connected using single MOS's drain node. At the condition of oscillation the amplitude of the signal is very easy to coupling to the substrate as shown in Fig. 5.

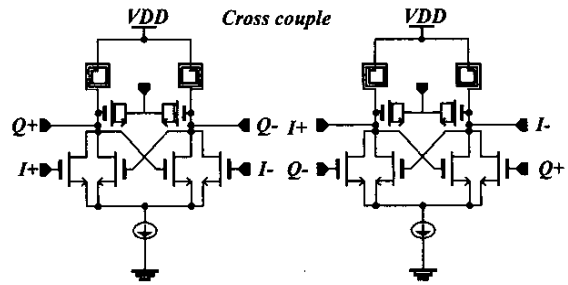

Fig. 4. Typical two cross-coupled VCO

In Fig. 5, Q of inductor, Q of varactor, and loss of drain of coupling MOS determine the total loaded Q of oscillator tank's node. The drain node of coupling MOS is connected to lossy silicon substrate which is very

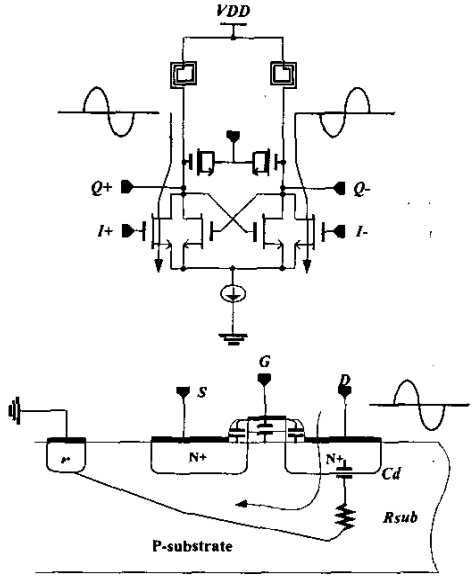

Fig. 5. Typical Quadrature VCO and its loss model

complicated and poor-modeled. This is modeled simply coupling capacitor and resistor which represents the substrate loss. To acquire high accurate and low phase noise characteristic of VCO, we remove this parasitic and uncertain connection. The proposed new quadrature VCO is shown in Fig. 6.

It consists of two identical LC oscillators M1-M8, which injection-lock to each other through coupling stages M9-M16. It can be shown that the output of two oscillators, QP-QN and IP-IN, always differ in phase by 90°. Furthermore, the synchronous oscillation frequency can be tuned with using the varactor (400f for one varactor) which is proposed in section 2. The square spiral inductors have 2nH (2T). This value offers good quality factor at operating frequency (5~6 GHz) and reasonable resonance frequency. For the realization of the negative resistance, the combination of nMOS and pMOS transistors, as can be found, e.g., in [11], was chosen as it reuses the dc current. Furthermore, the current source was omitted to maximize the signal swing. Omitting the current source has a few more advantages. It eliminates an important phase-noise source [12]. The main disadvantage of omitting the current source is the increased sensitivity to the power supply. This effect can be reduced by the cascode coupling n,pMOS.

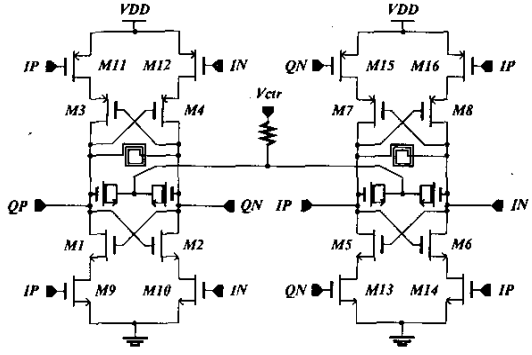

Fig. 6. Proposed new quadrature VCO

IV. MEASUREMENT

Fig. 7 (a) and (b) show the die-photograph and package on PCB of VCO. The fabricated chip photographs are shown in Fig. 7 (a) and (b) the chip size is 0.7mm×1.2mm. We package the chip using SSOP 24pin plastic package and for measurement, we use 2-layer FR4 PCB board. The

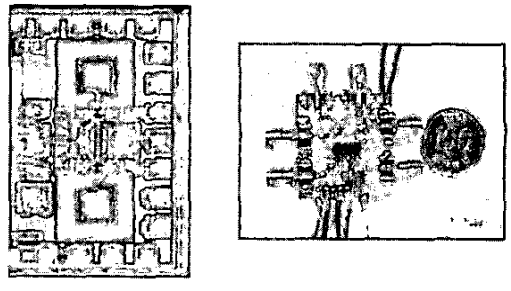

Fig. 7. (a) Die-photograph of quadrature VCO (b)Test package on PCB

buffer output (differential) is about −10dBm in a 50 Ω system. Total power consumption is 18mW (Two VCO core draws 3.2 mA and two output buffers 6.4 mA). Phase noise performance of the VCO has been measured using HP 8564E spectrum analyzer. Fig. 8 shows the spectrum of the VCO for a center frequency of 5.5 GHz. Phase noise @ 1MHz offset from the carrier is −115 dBc/Hz that meets the IEEE802.11a and HiperLAN type 2 requirements. The measured tuning characteristic of the

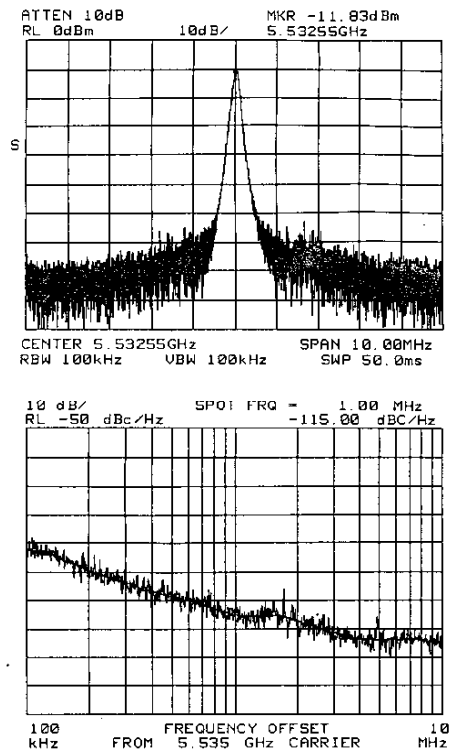

Fig. 8. Spectrum of the VCO at 5.5 GHz

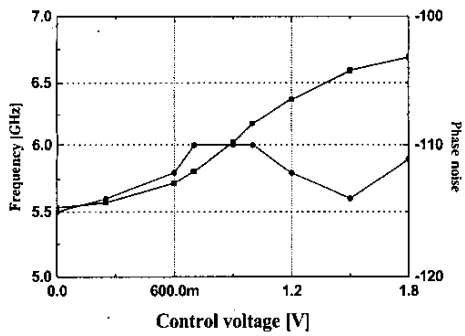

Fig. 9. Measured tuning characteristic & Phase noise at 100 MHz offse of the VCO

quadrature VCO is shown if Fig. 9. A tuning range of 1.2 GHz (5.4 ~ 6.6 GHz) is measured for control voltage variation from 0 to 1.8V.

CONCLUSION

A new low power low phase noise fully integrated CMOS quadrature LC VCO has been presented. The two VCO core consumes only 3.6 mW of power from a 1.8 V supply. The phase noise is –115 dBc/Hz @ 1 MHz offset from the 5.5 GHz.

ACKNOWLEDGEMENT

The authors wish to acknowledge the assistance of the RF CMOS team in ETRI.

REFERENCES

[1] P. R. Gray and R. G. Meyer et al., "Future directions in silicon IC's for RF personal communications," *Custom Integrated Circuits Conference*, 1995.

[2] A. A. Abidi et al., "The future of CMOS wireless transceivers, *Proc. IEEE Int. Solid-State Circuits Conf*, Feb 1997, pp. 118-119.

[3] H. S. Momose et al., "High-Frequency AC Characteristics of 1.5 nm Gate Oxide MOSFETs," *Proc. IEDM*, pp. 105-108, 1996.

[4] D. Su, et al., "A 5GHz CMOS transceiver for IEEE 802.11a Wireless LAN," *Proc. IEEE Int. Solid-State Circuits Conf*, pp. 92-93, Feb. 2002

[5] *IEEE 802.11a Physical Layer*, IEEE

[6] *Broadband Radio Access Networks: High Performance Radio Local Area Network Type 2*, ETSI TR 101-031

[7] P. R. Gray and R. G. Meyer, "Future directions in silicon IC's for RF personal communications," *Custom Integrated Circuits Conference*, 1995

[8] Thomas H. Lee, Hirad Samavati, and Hamid R. Rategh, "5-GHz CMOS Wireless LANs," *IEEE Trans. Microwave Theory Tech.*, vol. 50, no.1, pp. 268-279, Jan. 2002

[9] Q. Huang et al., "GSM Tranceiver Front-end Circuits in 0.25 μm CMOS," *IEEE J. Solid-State Circuits*, vol. 34, no. 3, pp. 292-303, March 1999.

[10] M. Rofougaran, A. Rofougaran, J. Rael, and A.A. Abidi, "A 900-MHz CMOS LC-oscillator with quadrature outputs," in *Proc. IEEE Int. Solid-State Circuits Conf.*, New York, NY, 1996, p. 392

[11] A. Hajimiri and T.H. Lee, "Design issues in CMOS differential LC oscillators," *IEEE J. Solid-State Circuits*, vol. 34, pp. 717-724, Feb. 1999.

[12] J.J. Rael and A.A. Abidi, "Physical processes of phase noise in differential LC-oscillators," in *Custom Integrated Circuits Conference*, Orlando, FL, May 2000, pp. 569-572.